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PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventor: JAN HAVEL

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COMPLETE SPECIFICATION

Electronic Multichannel Device for Sorting Coded Intelligence

We CESKOSLOVENSKA AKADEMIE VED, of No. 3, Marodni, Praha 1, Czechoslovakia, a Corporation of Czechoslovakia do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an electronic multichannel device for classifying or sorting information or intelligence coded in the form of a sequence of two types of electric pulses which is supplied to the input of the device corresponding to a digital intelligence expressed by an n-digit random number N in the binary system and achieving sorting of the digital intelligence in accordance with its numerical value into one of n intervals of adjustable width into which the entire range of the sequence of the set of the sorted intelligence or random numbers N is divided, the sorting of the intelligence being indicated by an electric pulse in one corresponding output of the n outputs of the said multichannel device.

Heretofore proposed devices have two channels and permit sorting of intelligence coded in the form of a sequence of two types of electric pulses supplied to its input into only one of two intervals of adjustable width. A sequence of two types of electric pulses which corresponds to a digital information expressed by an n-digit random number N in the binary system realises the sorting of the digital intelligence in accordance with its numerical value into one of two channels into which the total range of the set of sorted intelligence or random numbers N is divided. Sorting of the intelligence is indicated by an electric pulse in the corresponding (first or second) output of this two-channel device. Such a device may of course function not only as a two-channel sorting device, but it may also be used as a simple probability changer which, from a fundamental random independent pulse sequence of two types of electric pulses fed into the input of a two-channel device and corresponding to two different numbers, for example zero and one, with occurrence probability 0.5, forms a random independent sequence of electric pulses which is of the same type, but with adjustable probability, either $P(0)=p$ or $P(1)=1-p$.

The device in accordance with the invention can be operated not only as a multichannel electronic sorting device for sorting intelligence coded in the shape of a sequence of two types of electric pulses fed into its input, but also as a multiple probability changer which, in connection with a generator of electric pulses of two types whose occurrence probability equals 0.5, forms a so called generator of multinomic probability distribution, in whose n outputs or channels there appear electric pulses with a predetermined probability occurrence. The sum of the occurrence probabilities of the electric pulses in the individual output channels of the device equals 1. Such a device forms therefore a sequence of binomial random variables, or it simulates a new sequence of random variables each of which can achieve a certain number of values which is larger than 2 with stated probabilities whose sum equals 1.

The object of the device in accordance with the invention is to assist in the solution of many technical problems by means of statistic methods where it is very often necessary to generate random variables with a select-

[*Price* 4*s*. 6*d*.]

able value of probability, or it is necessary to sort numerical information or digital intelligence coded in the shape of a sequence of two types of electric pulses into a certain number of channels whose width and occurrence probability of the intelligence indicated therein can be predetermined. Though such operation can be carried out in universal digital computers, there occur under practical conditions cases where, for example, when carrying out measurement on industrial objects, under laboratory conditions in research work, universal digital computers cannot be used. In such and similar cases the device in accordance with the invention may be used for solving the above mentioned problem. By its dimensions, weight, simple attendance and service, and also by its price, it has the character of a laboratory instrument.

The present invention is an electronic multichannel device for sorting intelligence, coded as a sequence of two types of electric pulses, this sequence being supplied to the input of the device and representing a digital intelligence expressed by a n-digit random number N in the binary system, in accordance with its numerical value into one of n-intervals of adjustable width into which the entire range of the sequence of the set of the sorted intelligence or random numbers N is divided, in which device the sorting of the intelligence is indicated by an electric pulse in one corresponding output of the n-outputs of the said multi-channel device, the said multichannel device having two input terminals i.e. terminals serving for the input of pulses which correspond with the n-digit random number N in the binary system, the width of pulses supplying the first said input terminal of the device being different from the width of pulses being fed to the second input terminal of the device, said input terminals being connected in parallel with all corresponding input terminals of (n−1) logic circuits each of which operates in such a manner that on arrival of a pulse, corersponding to (1), at a first pair of terminals serving for the input of pulses to the logic circuit, which pulses correspond with the n-digit random number N in the binary system and, on arrival—at the same time—of a pulse, corresponding to (0), at a second pair of input terminals, which pulses corespond with a selectable n-digit number V_i in the binary system, a pulse corresponding to (1) occurs at the first terminal of a pair of output terminals of the logic circuit, while in all other combinations of input pulses a pulse corresponding to (0) occurs at the second of the pair of output terminals of the logic circuits, corresponding input terminals of a total of (2n−2) invertors being connected with the output terminals of the logic circuits mentioned above, which invertors reverse the polarity of pulses being fed into their inputs, and the output terminals of the invertors being connected in pairs as two inputs through which positive pulses are supplied to a total of (n−1) bistable flip-flop circuits, these (n−1) flip-flop circuits being basic reference-logic circuits of the value of the random number N and of a selectable number V_i in the binary system and—at the same time—storage elements which store intelligence about the result of the comparison until the next step, terminals serving for the supply of a clearing pulse into the total of (n−1) bistable flip-flop circuits being interconnected and connected with the source of a clearing pulse, and, next, outputs of the (n−1) bistable flip-flop circuits, which act as coincidence circuits and determine the corresponding interval $V_i \leq N < V_{i+1}$ and into which a negative pulse is fed through interrogation inputs connected in parallel after the comparison of the selectable number V_i and the random number N has been finished and, only in that case, if a small voltage occurs at the first of a pair of input terminals of the logic reference circuit belonging to the corresponding interval $V_i \leq N < V_{i+1}$ and, at the same time, if a large voltage occurs at the second of the pair of input terminals of the same logic reference circuit, then a pulse occurs in the output terminals of this logic reference circuit and, the first input terminal of the first logic reference circuit is connected with a source of D.C. voltage of a value U_1, which value U_1, for example, is smaller than a value of D.C. voltage U_2 of a source, with which is connected the second input terminal of the n-th logic reference circuit, the second input terminal of the first logic reference circuit being connected with the first output terminal of the first of the (n−1) bistable flip-flop circuits, next, the first input terminal of the second logic reference circuit is connected with the second output terminal of the first of the (n−1) bistable flip-flop circuits and, finally the first input terminal of the n-th logic reference circuit is connected with the second output terminal of the last i.e. of the (n−1)-th bistable flip-flop circuit, while output terminals of the n-logic reference circuits are connected with input terminals of n-gates preventing penetration of unwanted pulses which could arrive from the preceding circuits into the output circuits during the comparison between the random number N and the selectable numbers V_i and, therefore, the corresponding gate is conductive, i.e. is opened only in the period when a negative pulse arrives from the output of one of n-logic reference circuits to the input terminal of the corresponding gate, opening of the gates being controlled by positive suppressor pulses which are fed from a source, with which are connected corresponding input terminals of the gates connected in parallel, output terminals of which are connected with input termi-

nals of n-output monostable circuits and, therefore, a negative output pulse arriving from the corresponding gate is a trigger pulse which reverses its corresponding monostable circuit for the desired period and thus is created a positive output pulse of corresponding width in one of the n-outputs of the electronic multi-channel device for sorting coded intelligence.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Fig. 1 illustrates a block circuit for simulating a new sequence of random variables with predetermined probabilities, or a block circuit of an electronic multi-channel sorting device in connection with a source of coded intelligence;

Fig. 2 shows a simplified block circuit of the device in accordance with the invention;

Fig. 3 illustrates in more detail a block circuit of a device in accordance with the invention;

Fig. 4 shows an example of a circuit arrangement of one of the logic circuits employed;

Fig. 5 illustrates an example of a circuit arrangement of one of the inverters employed;

Fig. 6 shows an example of circuit arrangement of one of the bistable flip-flops employed;

Fig. 7 illustrates an example of a circuit arrangement of one of the logic reference circuits employed;

Fig. 8 shows an example of a circuit arrangement of one of the gates employed;

Fig. 9 illustrates an example of a circuit arrangement of one of the monostable output circuits employed; and

Fig. 10 shows the time sequence of the suppressor, interrogation and clearing pulses.

Referring now more particularly to the Figures, it should be understood from Fig. 1 that the block 01 represents a generator or a source in whose output 010 there appears a basic random independent sequence of the two types of pulses, corresponding for example to 0 and 1, with an occurrence probability 0.5, this pulse sequence or train corresponding to a 10-digit random number N in the binary system. The output 010 is connected with the input of an electronic multi-channel device for sorting intelligence or with the input of a multi-channel probability changer 02 whose ten outputs are designated 10,20 to 100.

Fig. 2 illustrates in more detail the block circuit of the device in accordance with the invention. The input 010 of the pulses corresponding to 1 and 0 is branched off to all nine simple probability changers, or two-channel electronic intelligence classifiers or sorters 1, 2 to 9. The input 13 of the clearing pulse is also led to all sorters 1 to 9. The group of nine two-channel sorters 1 to 9 forms the first part of the device in accordance with the invention. The outputs of the two-channel sorters 310 to 390 are connected with the inputs of the block 03 which illustrates the second part of the device in accordance with the invention. This second part shapes the output voltage of the first part into the required final shape. The corresponding outputs are designated 10, 20 to 100 (a total of ten outputs). The input 11 is supplied with a d.c. voltage U1, the input 12 is supplied with a voltage U2, U1 being smaller than U2. The input 14 is supplied with interrogation pulses, and the input 15 is supplied with suppressor pulses. The employed nine two-channel information sorters produce 9 selectable numbers V_1 to V_9, there being created ten partial intervals from the fundamental interval 0 to 1, and ten channels with ten outputs. If there is required a larger number of partial intervals, the number of two-channel information sorters and the number of corresponding members in the block 03 are increased. For example, for twenty intervals it is necessary to employ nineteen two-channel sorters and to form twenty channels with the corresponding number of members of the block 03 with twenty outputs.

Fig. 3 illustrates in more detail the block circuit of the device in accordance with the invention. The terminals 111 and 112 are input terminals for supplying pulses corresponding to a ten-digit random number N in the binary system, the width of the pulses N—1 which reach the terminals 111 and the width of the pulses N—2 which reach the terminal 112 being of a different width. The terminals 211, 212, 221, 222 to 291, 292 are input terminals for the supply of pulses for a selectable number Vi in the binary system, the width of the pulses Vi—1 which reach the terminals 211, 221 to 291 and the width of the pulses Vi—2 which reach the terminals 212, 222 to 292 being again different.

The upper half of the block circuit represents the first part of the device. It is formed by logic circuits of two-channel intelligence sorters connected in parallel. Each of the two-channel sorters is formed by one logic circuit of the row 31 to 39, of two inverters of the row 41 to 49, and of one bistable flip-flop of the row 51 to 59.

The lower half of the block circuit represents the second half of the device and it is formed by rows of logic circuits 601 to 610 connected in parallel, gates 701 to 710, and monostable output circuits 801 to 810. The outputs of the device in accordance with the invention are designated 1 to 10. The terminal 11 is supplied with a d.c. voltage U1, the terminal 12 is supplied with a d.c. voltage U2. The terminal 13 is supplied with a voltage for clearing the flip-flops 51 to 59,

that is setting them to zero position, and the terminal 14 is supplied with an interrogation pulse into the logic circuits 601 to 610, and the terminal 15 is supplied with a suppressor pulse into the gates 701 to 710.

Fig. 4 illustrates an example of the circuit arrangement of one group of logic circuits 31 (of Fig. 3). The input terminals are 111, 211, 212 and 112, the output terminals are 311 and 312. The input terminal 111 is supplied with pulses 1 and the terminal 112 with pulses 0 corresponding to a ten-digit number N in the binary system. The widths of the pulses on the terminals 111 and 112 are different. The input terminals 211 and 212 are fed, synchronously with pulses corresponding to a random number N, with pulses corresponding to a selectable ten-digit number Vi in the binary system. The widths of these pulses on the terminals 211 and 212 are again different like in the case of the pulses of the random number N. In the circuit there are used two transistors 03 and 04 and other currently employed components, that is resistors and capacitors. The terminal 01 is grounded and connected with the positive terminal of the supply source, the terminal 02 is connected with the negative pole of this source. The electric output pulses are led through the terminals 311, 312 into two inverters 41 (of Fig. 5) which invert their polarity.

Fig. 5 illustrates the circuit arrangement of one of the inverters of the row 41 to 49 which reverses the polarity of the pulse. The circuit comprises a transistor 03 and other currently employed components. The input terminal is 311, the output terminal is 411; the terminal 01 is connected with the positive pole of the source and grounded, the terminal 02 is connected with the negative pole of this supply source. The input terminal 311 is supplied with negative pulses, positive pulses leave the output terminal 411.

Fig. 6 illustrates the circuit arrangement of one of the bistable flip-flops of the row 51 to 59 which is the fundamental reference circuit of the value of the random number N and the selectable number Vi. This circuit is also a storage element which stores intelligence about the result of the comparison until the next stop.

The bistable flip-flop 51 has input terminals 411 and 412 and output terminals 511 and 512. The terminal 13 serves for the supply of a clearing pulse, the terminal 01 is connected with the positive pole of the supply source and grounded, the terminal 02 is connected with the negative pole of this source. The circuit comprises two transistors 03 and 04, two rectifiers 015 and 016, and the currently employed components. The pulses reaching the input terminal 411, 412 are positive.

Fig. 7 illustrates the circuit arrangement of one of the logic reference circuits 601 to 610 which operate as coincidence circuits and determine the respective interval Vi—N Vi—1. After terminated comparison between the numbers Vi and N, an interrogation pulse is supplied to the circuits 601 to 610 into the input 14. 6011 and 6012 are input terminals, 061 is the output terminal. The terminal 01 is connected with the positive pole of the supply source and it is also connected with ground, the terminal 02 is connected with the negative pole of this source. Each of the logic circuits 601 to 610 comprises two transistors 03 and 04, one rectifier 09, and also the other currently employed components. The transistors are connected as emitter followers. In the output terminal 061 there appears a pulse only if a (negative) interrogation pulse reaches the terminal 14 and if, at the same time, there is a small voltage on the terminal 6011 and a large voltage on the positive terminal 6012. The pulse on the output terminal 061 of the logic circuit reserved for the respective interval advances into the gate 701 (of Fig. 6).

Fig. 8 illustrates the circuit arrangement of one of the gates of the row 701 to 710 which prevents penetration of unwanted pulses which could arrive from the preceding circuits into the output circuits during the comparison between the number N and the numbers Vi. The gate 701 is therefore conductive only in the period when a negative pulse arrives from the circuit 601 to the input terminal 7011. Opening of the gates is controlled by positive suppressor pulses which reach the terminal 15. The output terminal is designated 071; the terminal 01 is grounded and it is connected with the positive terminal of the supply source; the terminal 02 is connected with the negative pole of this source. The output pulse on the terminal 071 is negative. The circuit comprises a transistor 03 and other currently employed components.

Fig. 9 illustrates the circuit arrangement of one of the monostable output circuits 801 to 810. The input terminal is designated 8011, the output terminal is designated 081; the terminal 01 is grounded and also connected with the positive pole of the supply source; the terminal 02 is connected with the negative pole of this source. There are two transistors which are designated 03 and 04. There are also other currently employed circuit components. The pulse which passes through the gate 701 (of Fig. 8) and reaches the input terminal 8011 as a trigger pulse is a negative one and reverses the position of the circuit 801 for a period determined by the magnitude of the capacitor 09. This creates a positive output pulse of corresponding width on the terminal 081.

Fig. 10 illustrates the time sequence of the suppressor interrogation and clearing pulses.

In the left part of the Figure there is illustrated a sequence of ten or eleven pulses, that is the first to tenth pulse, and the following first pulse of the next ten pulses forming a random ten-digit number N. In the interval after termination of the tenth, and before beginning of the next first pulse corresponding to a random number N, that is in the interval 20, there is produced in the period 21 a positive suppressor pulse 15. The negative interrogation pulse 14 follows after the beginning of the pulse 15 after a time 22. After termination of the interrogation pulse 14, there arrives a clearing pulse 13 whose leading edge is in the same position on the time axis as the trailing edge of the interrogation pulse 14. The pulse 13 is of course not made use of; use is only made of its derivative 013 which lies in the same position on the time axis as the trailing edge of the pulse 13.

The object and the operation of the device in accordance with the invention can be clearly and comprehensively explained by means of an example of its application in solving a problem relating to the simulation of random variables each of which may assume more than two values with predetermined probabilities whose sum equals 1.

Consider a die; each cast, that is each realisation gives one value, names one of six possible numbers 1 to 6. Chance decides which of the mentioned numbers it will be and all numbers have in the case of this die the same probability. The so called generator of multinomic probability distribution simulates the operation of a generalised die. At each case, that is at each realisation, there is created in its output a certain value of the total number of n possible values, where for example $2 \leq n \leq 10$, and each value has a predetermined occurrence probability. The probability can therefore be expressed by the following expression:— $P/h_1/=p_1$, $P/h_2/=p_2$, $P/h_n/=p_n$, and further $\sum_{i=1}^{n} p_i=1$ where h designates a certain value of the total number of n possible values created across the generator output. Each probability p_i can be adjusted within the range $2^{-10} \leq p_i \leq 1$ by steps of a value 2^{-10}. If the random variable ξ has a value X_j, j being equal to 1, 2, . . . n, with a probability $P(\xi=X_j)=p_j$, and if $\sum_{J=1}^{n} P_J=1$, then the multinomic distribution of the probability is the distribution of the number of values X_i in the sequence of random variables $[\xi_i, i=1, 2, \ldots]$. The device in accordance with the invention can simulate this type of a random variable.

The device in accordance with the invention operates in the following manner:

Into all two-channel sorters there arrives from the source of coded intelligence through the terminal 111 and 112 a common ten-digit binary random number N. Into each of the two-channel sorters there arrives synchronously with the number N also a so called selectable number Vi created in the auxiliary circuits which form a part of each two-channel sorter. Both numbers N and Vi reach values only within a certain interval; in the case considered the extreme limits are the numbers "0 0 0 0 0 0 0 0 0 0" and "1 1 1 1 1 1 1 1 1 1". For a correct function of the device it is necessary to meet the condition that the numbers "$V_i(i=1, 2 \ldots 9)$" must satisfy unequality no. 1:

$$0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \leq V_1 \leq V_2 \leq \ldots \leq V\,9 \leq 1\,1\,1\,1\,1\,1\,1\,1\,1\,1.$$

The value V_i is a selectable number for the first sorter with input terminals 211 and 212. The number N is the single one which is in common for all sorters. The number V_i belongs only to the i-th sorter. The selection of the number V_i determines the width of the interval, or the value of the probability in the corresponding channel. In each sorter the entire numerical interval is always divided into two partial intervals, namely:

$$(0\,0\,0\,0\,0\,0\,0\,0\,0\,0 - V_i) \text{ and } (V_i - 1\,1\,1\,1\,1\,1\,1\,1\,1\,1)$$

The length of these intervals is directly proportional to the respective probabilities p_i and $(1-p_i)$. This follows from the fact that the probability of all possible values of the numbers N is the same, the numbers N being uniformly distributed over the interval 0 to 1. If the unequality no. 1 is satisfied, is is obvious that the first interval $(0\,0\,0\,0\,0\,0\,0\,0\,0\,0 - V_i)$ is progressively increased in the sorters and in each following sorter there is also a larger probability p_i.

The operation of the sorter resides substantially in the fact that one compares the value of the random number N against the value of the selectable number V_i, and in accordance with the fact which of the unequalities

$$N \geq V_i, \quad N < V_i$$

is satisfied one obtains in the first and second output an intelligence with a corresponding probability p_i or $(1-p_i)$. All parallel connected two-channel sorters or probability changers work in this manner. Since there is a single random number which is the same for all sorters and since the selectable numbers satisfy the above mentioned unequality no. 1, there appears the following situation with a certain number N

if $N \geq V_i$, there appears a pulse A,

if $N < V_i$, there appears a pulse B in the

sorter outputs, so that in the row of the outputs of the bistable flip-flops 51 to 59 there is, for example, produced the following pulse train:

"A A A B B B B B B".

The remaining part of the device operates in the following manner: The numerical interval 0 to 1 is divided by selectable numbers V_i into a series of partial intervals and the sorters or the probability changers accomplish evaluation of the following unequality no. 2:

$$O \leq N < V_1 \leq N < V_2 \leq \ldots V_8 \leq N < K,$$

K being larger than 1. It is necessary to consider $K>1$ to satisfy the condition $0 \leq p_i \leq 1$. In the preceding unequality no. 2, the lengths of the individual partial intervals limited by the numbers V_i and V_i+1 correspond to the respective probabilities p_i, and since the number N is the only one, the following unequality no. 3:

$$V_i \leq N < V_{i+1}$$

will be satisfied only in one case. The further part of the device indicates therefore the interval in which just this unequality no. 3 has been satisfied. In a two-channel sorter it is the flip-flop which determines whether an unequality of the first or of the second type has been satisfied. The flip-flop is set to one or the other position; if one follows the voltage at one output point, for example on the first anode in the case of a tube circuit, or on the first collector in the case of a transistor circuit, there is at this point in the first case a voltage U1, and in the second case there is a voltage U2, U1, being smaller than U2, or

if $N \geq V_i$, the voltage U1 is indicated, and if $N < V_i$, the voltage U2 is indicated.

It follows from the above mentioned unequality no. 2 that in order to obtain ten possible partial intervals from the fundamental interval /O, K>1/, nine selectable numbers V_i and therefore nine common sorters i.e. simple sorters or changers of probability are required. The extreme points of the interval 0, K are invariable, that is, at their place one obtains always a constant result, that is

if $O \leq N$, the output voltage is U1, and if $K > N$, the output voltage is U2.

The voltages in the sorter output, that is in the output of the bistable flip-flops 51 to 59, can therefore produce the following arrangement only:

U1	U2	U2	U2	U2	U2	U2	U2	U2	U2	U2
U1	U1	U2	U2	.	.	.	U2	U2	U2	U2
U1	U1	U1	U2	U2	.	.	.	U2	U2	U2
U1	U1	U1	.	.	.	U1	U1	U1	U2	U2
U1	U1	U1	U1	U1	U1	U1	U1	U1	U1	U2

In all cases the partial interval sought for is the one which lies on the boundary of the voltages (U1—U2). Intervals on the boundary of the voltages of the same type (U1—U1) or (U2—U2) do not satisfy the condition

$$V_i \leq N < V_{i+1}.$$

The output voltage appears therefore only in the channel which corresponds to the interval (U1—U2) and which, consequently, satisfies the condition $V_i \leq N < Vi+1$.

If one selects the number $V_i = V_{i+1}$, both two-channel sorters or simple probability changers will always give the same result, and this interval has therefore zero length. One may therefore proceed in the same manner if one requires division of the fundamental interval into a small number of partial intervals than the maximum usable number of ten, that is the simulated random variable can assume a smaller number of values.

The voltage values U1 or U2 are obtained from the individual bistable flip-flops 51 to 59 which form part of the two-channel sorters or simple probability changers. These voltages are fed into the logic circuits 601 to 610 whose task it is to indicate the case of a difference, that is the existence of a difference (U1—U2). Into the first logic circuit 601 one feeds on the one hand the constant voltage U1 from the terminal 11 (corresponds to the beginning of the fundamental interval $O \leq N$), on the other hand the output voltage from the flip-flop 51. Into the second logic circuit 602 one feeds analogically on the one hand the output voltage from the flip-flop circuit 51, on the other hand the output voltage from the flip-flop circuit 52. Finally, the last interval, in the case considered the tenth, is indicated by the logic circuit 610 into which is fed on the one hand the output voltage from the last sorter, that is the output voltage from the flip-flop 59, on the other hand the constant voltage U2 from the terminal 12 corresponds to the end of the fundamental interval $K > N$.

After termination of the evaluation of the unequality

$$N \geq V_i, \qquad N < V_i$$

in the individual two-channel sorters there arrives from the terminal 14 an interrogation

pulse into the logic circuits 601 to 610; the interrogation pulse enters the output only in the single logic circuit into which there arrives on the one hand the voltage U1, on the other hand the voltage U2. In all other logic circuits 601 to 610 both voltages have the same value U1 or the same value U2, and there appears therefore in the output of these logic circuits no pulse. The output pulse, for example from the output of the logic circuit 603, passes further through the respective gate 703, which, at this moment, is made conductive by the suppressor pulse arriving from the terminal 15. The circuits 701 to 710 act as gates whose task it is to prevent parasitic pulses from penetrating into the output circuits 801 to 810. The parasitic pulses could be formed during the evaluation process in the flip-flops 51 to 59 and could be further transmitted through the logic circuits 601 to 610 into the end circuits. Therefore, the suppressor pulse arriving from the terminal 15 opens the gates only at the moment at which there exists the possibility of an interrogation pulse arriving from the terminal 14 through the logic circuit 601 to 610. The pulse in the output of one gate 701 to 710 triggers the respective output circuit (one of 801 to 810) which produces in this channel an output pulse.

After evaluation terminated by the flip-flops 51 to 59, the latter are cleared by a clearing pulse supplied from the terminal 13. Clearing brings the flip-flops 51 to 59 into the starting position.

On arrival of pulses corresponding to the number "1" or "0" on the terminals 111, 212, and 211, 112, the logic circuits 31 to 39 perform the following operations:

111		212		311	211		112		312
1	+	1	=	0	1	+	1	=	0
1	+	0	=	1	1	+	0	=	1
0	+	1	=	0	0	+	1	=	0
0	+	0	=	0	0	+	0	=	0

That means that a pulse (1) appears on the output terminal 311 only if on the terminal 11 there is a pulse (1), and on the terminal 212 there is a pulse (0). In the other cases there appears no pulse on the output terminal, that is the logic circuit between the terminals 111 and 311 is not conductive. The logic circuit between the terminal 211 and 312 acts in a similar manner.

Since the numbers are progressively compared from the lowest one to the highest, it is sufficient for the device to store the result of comparison only until the nearest step. If there occurs therein a change against the past, only this change has an influence at this moment. In order to make the function of the bistable circuit correspond to the above mentioned requirements, it is necessary to supply to two independent inputs 411 and 412 a selectable and random number not directly, but through the logic circuits 31 to 39 (of Fig. 4) and through the terminals 41 to 49 (of Fig. 5). After comparison on the highest order of the number there occurs evaluation and clearing of the bistable flip-flop 51, that is this circuit is brought into a position corresponding to the starting position $N \geq V_i$. The output 511 of the circuit 51 is connected to the input 6012 of a logic coincidence circuit 601 (of Fig. 7), and the output 512 of the circuit 51 is connected with the input 6021 of another logic coincidence circuit 602.

The circuit arrangement may be changed without changing the function.

The device in accordance with the invention may be used in addition to the above described method, that is as a sorting device, particularly also when solving technical problems by statistic methods where it is necessary to simulate or to generate random variables with a selectable value of the probability occurrence.

WHAT WE CLAIM IS:—

1. An electronic multi-channel device for sorting intelligence, coded as a sequence of two types of electric pulses, this sequence being supplied to the input of the device and representing a digital intelligence expressed by a n-digit random number N in the binary system, in accordance with its numerical value into one of n-intervals of adjustable width into which the entire range of the sequence of the set of the sorted intelligence or random numbers N is divided, in which device the sorting of the intelligence is indicated by an electric pulse in one corresponding output of the n-outputs of the said multi-channel device, the said multi-channel device having two input terminals i.e. terminals serving for the input of pulses which correspond with the n-digit random number N in the binary system, the width of pulses supplying the first said input terminal of the device being different from the width of pulses being fed to the second input terminal of the device, said input terminals being connected in parallel with all corresponding input terminals of $(n-1)$ logic circuits each of which operates in such a manner that on arrival of a pulse, corresponding to (1), at a first pair of terminals serving for the input of pulses to the logic circuit, which pulses correspond with the n-digit random number N in the binary system and, on arrival—at the same time—of a pulse, corresponding to (0), at a second pair of input terminals, which pulses correspond with a selectable n-digit number V_i in the binary system, a pulse corresponding to (1) occurs at the first terminal of a pair of output terminals of the logic circuit, while in all other combinations of input pulses a pulse corresponding to (0) occurs at the second,

of the pair of output terminals of the logic circuits, corresponding input terminals of a total of (2n−2) invertors being connected with the output terminals of the logic circuits mentioned above, which invertors reverse the polarity of pulses being fed into their inputs, and the output terminals of the invertors being connected in pairs as two inputs through which positive pulses are supplied to a total of (n−1) bistable flip-flop circuits, these (n−1) flip-flop circuits being basic reference-logic circuits of the value of the random number N and of a selectable number V_i in the binary system and—at the same time—storage elements which store intelligence about the result of the comparison until the next step, terminals serving for the supply of a clearing pulse into the total of (n−1) bistable flip-flop circuits being interconnected and connected with the source of a clearing pulse and, next, outputs of the (n−1) bistable flip-flop circuits are connected with inputs of a total of n-logic reference circuits, which act as coincidence circuits and determine the corresponding interval $V_i \leq N < V_{i+1}$ and into which a negative pulse is fed through interrogation inputs connected in parallel after the comparison of the selectable number V_i and the random number N has been finished and, only in that case, if a small voltage occurs at the first of a pair of input terminals of the logic reference circuit belonging to the corresponding interval $V_i \leq N < V_{i+1}$ and, at the same time, if a large voltage occurs at the second of the pair of input terminals of the same logic reference circuit, then a pulse occurs in the output terminals of this logic reference circuit and, the first input terminal of the first logic reference circuit is connected with a source of D.C. voltage of a value U_1, which value U_1, for example, is smaller than a value of D.C. voltage U_2 of a source, with which is connected the second input terminal of the n-th reference circuit, the second input terminal of the first logic reference circuit being connected with the first output terminal of the first of the (n−1) bistable flip-flop circuits, next, the first input terminal of the second logic reference circuit is connected with the second output terminal of the first of the (n−1) bistable flip-flop circuits and, finally the first input terminal of the n-th logic reference circuit is connected with the second output terminal of the last i.e. of the (n−1)-th bistable flop-flop circuit, while output terminals of the n-logic reference circuits are connected with input terminals of n-gates preventing penetration of unwanted pulses which could arrive from the preceding circuits into the output circuits during the comparison between the random number N and the selectable numbers V_i and, therefore, the corresponding gate is conductive, i.e. is opened only in the period when a negative pulse arrives from the output of one of n-logic reference circuits to the input terminal of the corresponding gate, opening of the gates being controlled by positive suppressor pulses which are fed from a source, with which are connected corresponding input terminals of the gates connected in parallel, output terminals of which are connected with input terminals of n-output monostable circuits and, therefore, a negative output pulse arriving from the corresponding gate is a trigger pulse which reverses its corresponding monostable circuit for the desired period and thus is created a positive output of corresponding width in one of the n-outputs of the electronic multi-channel device for sorting coded intelligence.

2. An electronic multi-channel device substantially as hereinbefore described with reference to the accompanying Figs. 1 to 10.

H. D. FITZPATRICK & CO.,
Patent Agents,
5 Park Gardens, Glasgow, C.3.
and
3 Grays Inn Square, London, W.C.1.

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1151377 COMPLETE SPECIFICATION
9 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

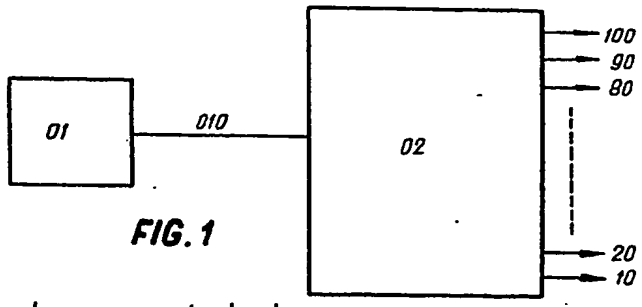

FIG. 1

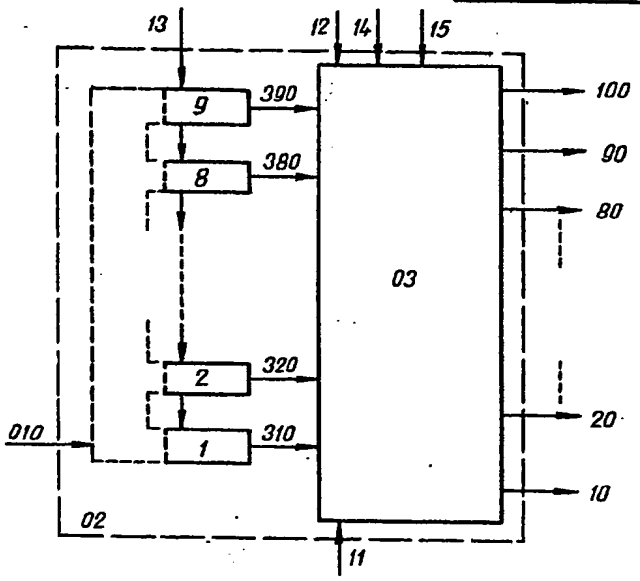

FIG. 2

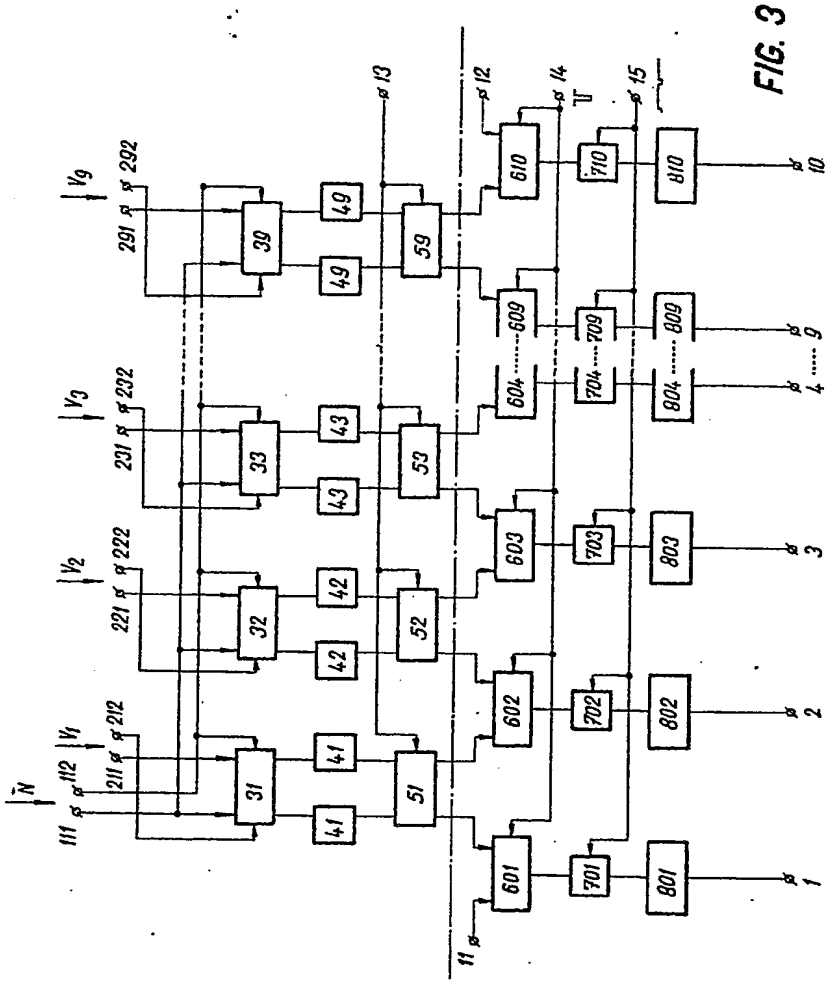

FIG. 3

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Sheets 2 & 3

FIG. 3

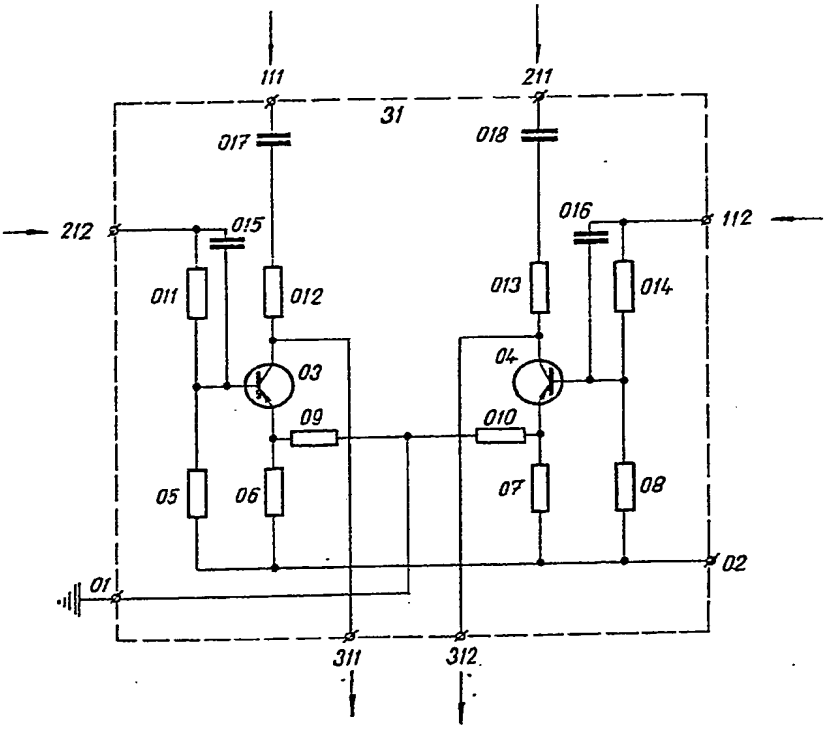

FIG. 4

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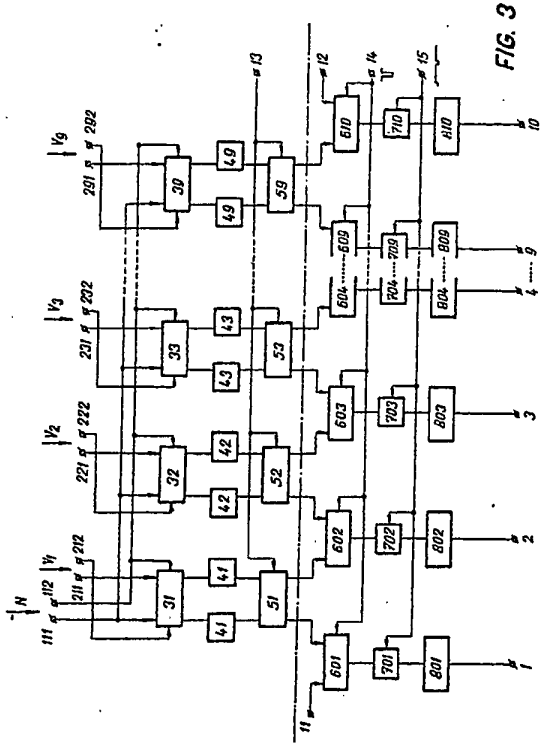

FIG. 3

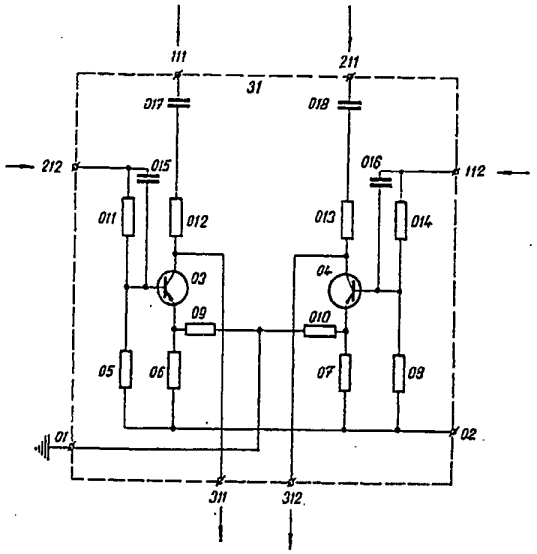

FIG. 4

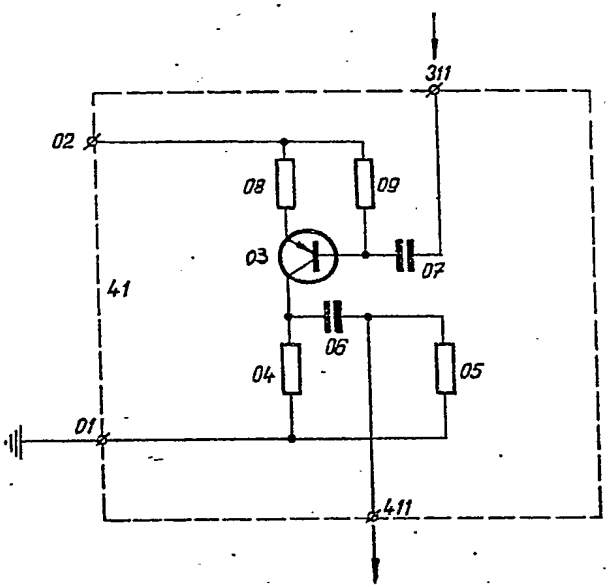

FIG. 5

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Sheets 4 & 5

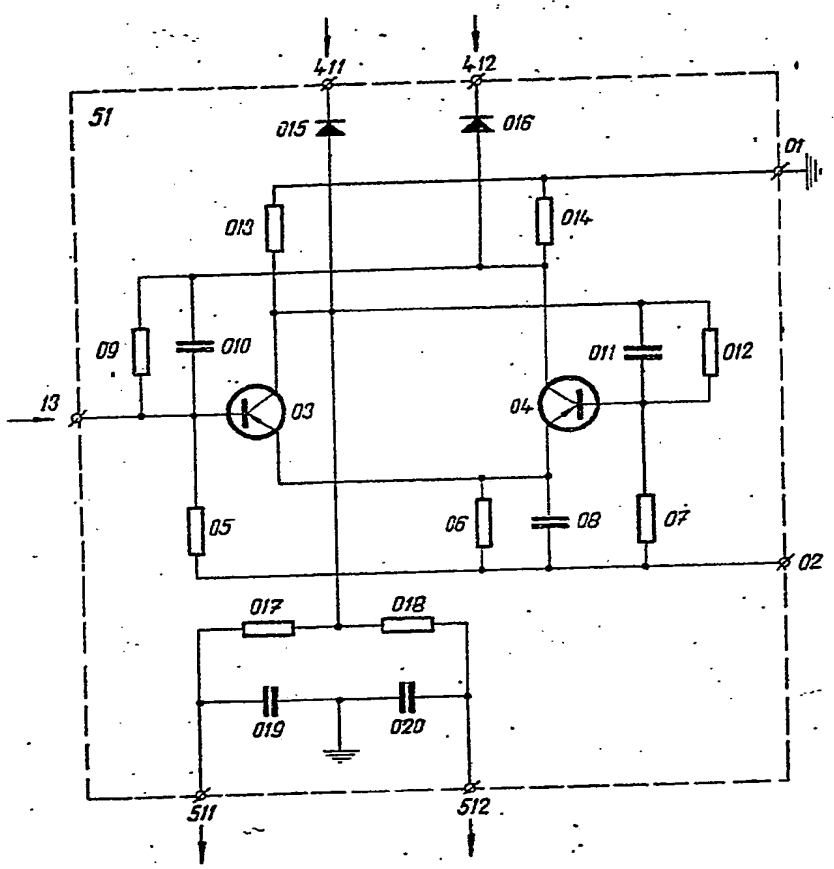

FIG. 6

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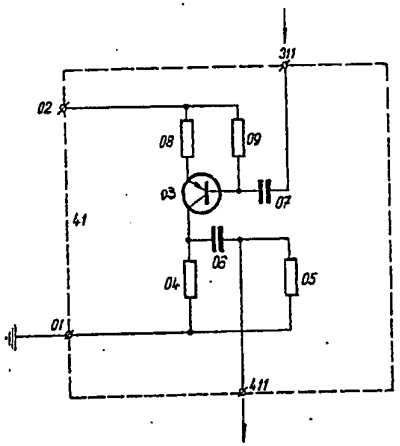

FIG. 5

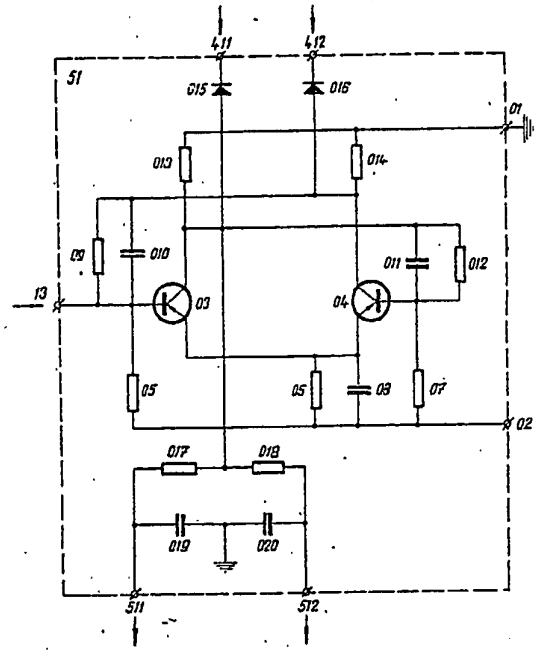

FIG. 6

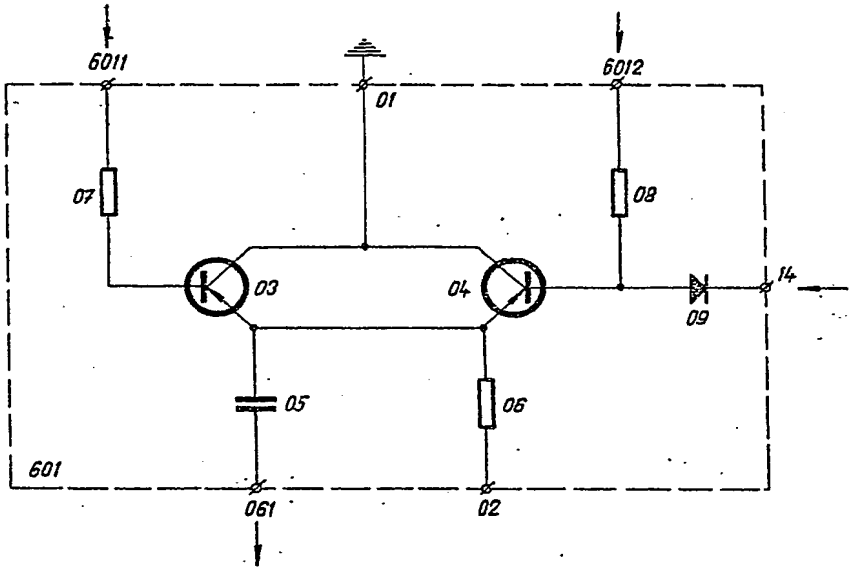

FIG. 7

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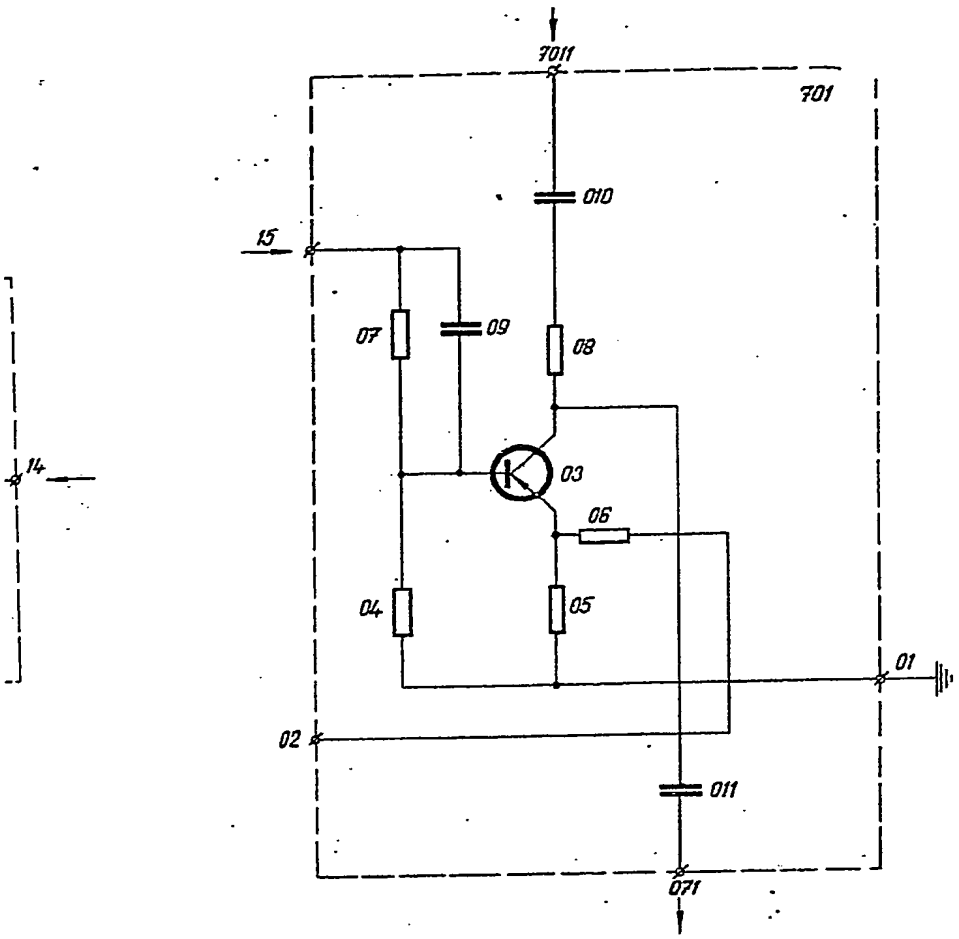

FIG. 8

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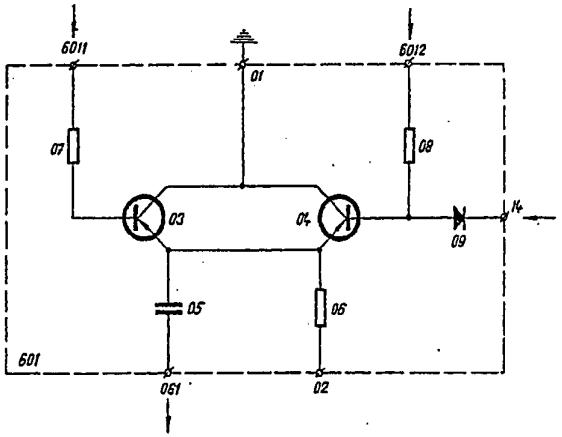

FIG. 7

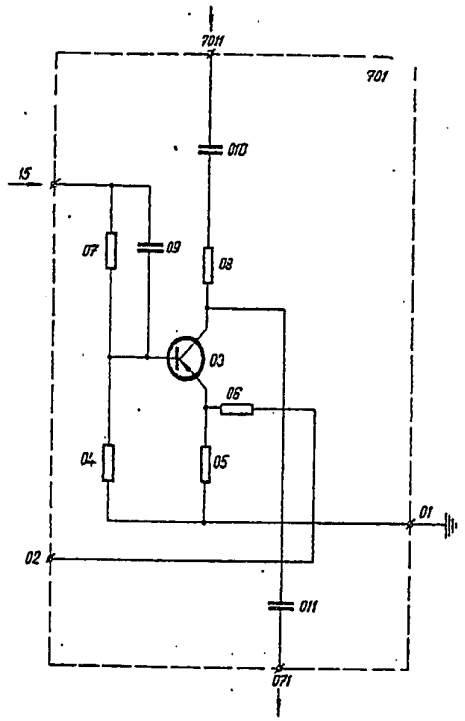

FIG. 8

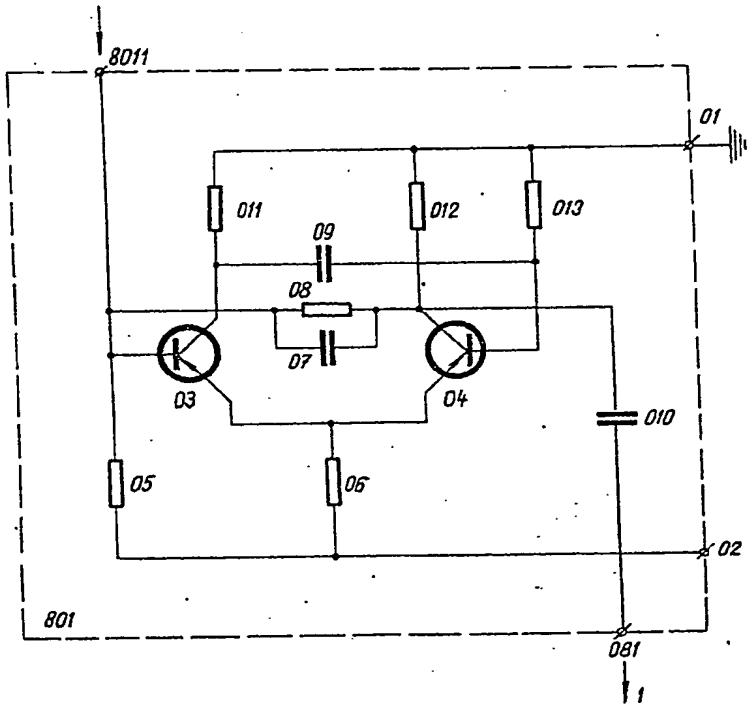

FIG. 9

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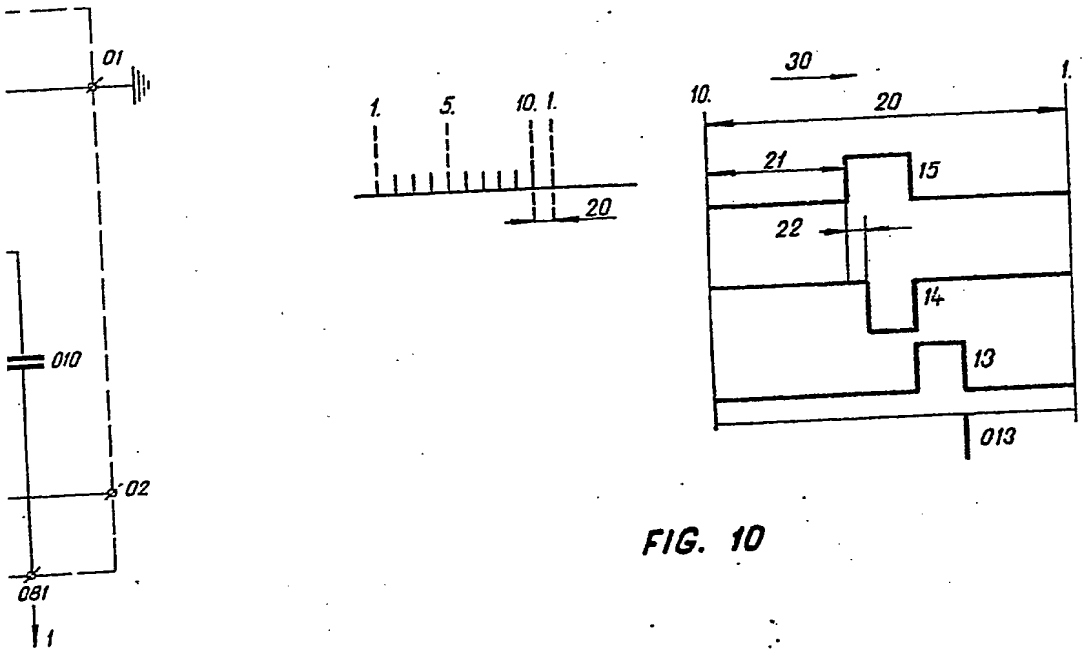

FIG. 10

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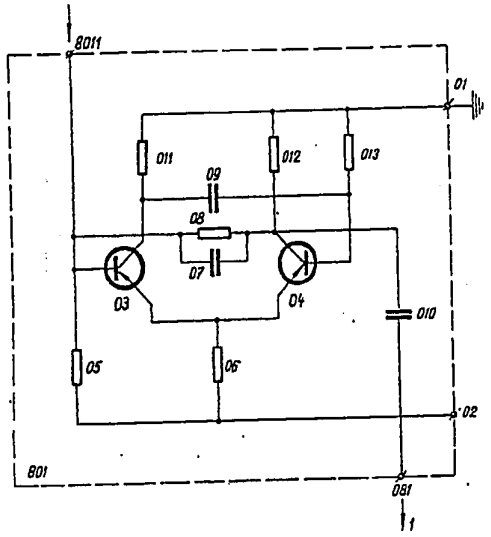

FIG. 9

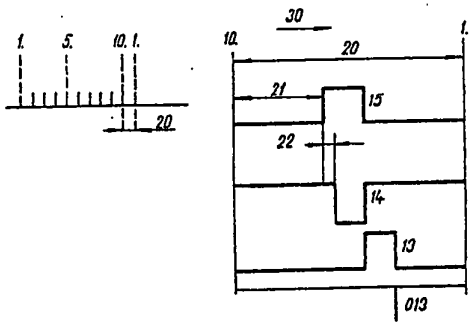

FIG. 10